IN THE CLAIMS

1. (Currently amended) A method for writing data from a processor to a non-volatile memory embedded in an integrated circuit using an interface circuit, comprising the following steps:

_____ (a) said interface circuit intercepting access of the processor to the non-volatile memory for writing data to the non-volatile memory, causing at least part of said data to be written to said non-volatile memory to be is transferred instead to a volatile memory,

_____(b) when said data has been transferred to said volatile memory-, the interface circuit sending a wait signal is-sent-to said processor-,

_____-(c) the interface circuit transferring said part of said data is-transferred-from said volatile memory to said non-volatile memory, and

_____(d) said-the interface circuit removing the wait signal (wait) is removed.

2. (Canceled)

3. (Currently amended) The method for writing data according to claim 1, wherein at the beginning of the data transfer from the volatile memory to the non-volatile memory-, said non-volatile memory is set in write mode.

4. (Previously presented) The method for writing data according to claim 1, wherein during the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in program mode.

2

5. (Previously presented) The method for writing data according to claim 1, wherein at the end of the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in read mode.

6. (Currently amended) The method for writing data according to claim 1, wherein all of the data is transferred first to the volatile memory.

7. (Previously presented) The method for writing data according to claim 1, wherein the addresses corresponding to the data to be written to the non-volatile memory are stored intermediately.

8. (Previously presented) The method for writing data according to claim 1, wherein before the data is written to the volatile memory, the wait signal is sent to the processor and is removed after said data is completely written to said volatile memory.

9. (Canceled)

10. (Currently amended) The integrated circuit according to claim 13,9, wherein the non-volatile memory is a flash memory.

11. (Currently amended) The integrated circuit according to claim 13,9, wherein the volatile memory is a random access memory or a static random access memory.

3

12. (Currently amended) The integrated circuit according to claim 139, wherein the volatile memory is an embedded volatile memory.

13. (New) An integrated circuit comprising:

a processor;

a non-volatile memory embedded in the integrated circuit and coupled to said processor;

an interface circuit coupled to the processor and to the non-volatile memory, wherein said interface circuit:

(a) intercepts access of the processor to the non-volatile memory for writing data to the non-volatile memory, causing at least part of said data to be written to said non-volatile memory to be transferred instead to a volatile memory;

(b) sends a wait signal to said processor when said data has been transferred to said volatile memory;

(c) transfers said part of said data from said volatile memory to said non-volatile memory, and

(d) removes the wait signal.

4